AMENDMENTS

This section presents changes to the specification and the claims in a clean-unmarked format. A version with markings to show the changes made by the current amendment is provided after the remarks section.

In The Specification:

Please replace the paragraph beginning at page 12, line 16 with the paragraph:

Fig. 5 is a block diagram illustrating a particular embodiment of a transaction generator 20 in accordance with the present invention. The embodiment of Fig. 5 implements the transaction generator 20 with an Intel® Pentium® Pro processor bus. While Fig. 5 illustrates an implementation of the transaction generator 20 with the Pentium® Pro processor bus, the present invention is not limited to any particular type of bus. It would be well within the ordinary skill in the art to apply the present invention to other bus types by one in the art having the benefit of this disclosure. In the exemplary embodiment of Fig. 5, the logic device 25 comprises three field programmable gate arrays (FPGA) 50, 52, 54. Suitable FPGAs, for example, include model 4036XL or 4062XL FPGAs available from Xilinx® Inc., San Jose, CA. The FPGAs 50, 52, 54 may be programmed using a hardware descriptive language as is known in the art, such as VHDL or Verilog. Alternately, application specific integrated circuits (ASIC) may be designed, or discrete logic devices may be arranged, to implement the digital logic functions of the transaction generator 20 by one skilled in the art having the benefit of this disclosure.
